Oracle SPARC T4 and T3 Servers’ Differences

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Overview of the SPARC T4 and SPARC T3 Servers

The SPARC T4 based servers consists of the SPARC T4-1, SPARC T4-2 and SPARC T4-4 rack mount servers along with the SPARC T4-1B server blade displayed in figures 1a -1d. They use the same chassis (Sun Blade 6000 A90-B or A90-D) as their predecessors, the SPARC T3 Servers. These servers are made up of the SPARC T3-1, SPARC T3-2 and SPARC T3-4 rack mount servers along with the SPARC T3-1B server blade.

NOTE: Throughout this document you will be referenced to the platform’s technical documentation. Listed here are the links to this documentation that will be active once the SPARC T4 Servers release.

T4-1: http://download.oracle.com/docs/cd/E22985_01
T4-2: http://download.oracle.com/docs/cd/E23075_01
T4-4: http://download.oracle.com/docs/cd/E23411_01
T4-1B: http://download.oracle.com/docs/cd/E22735_01
NOTE: If you are not familiar with the SPARC T3 servers it is highly recommended that you review the SPARC T3 based servers course that can be accessed through this link (http://ilearning.oracle.com/ilearn/en/learner/jsp/rcd_details_find.jsp?rcoid=927425588) before you continue this differences document.

Physical Differences between the SPARC T4 and T3 Servers

The SPARC T4 Servers are physically the same as their SPARC T3 predecessors. One exception is the SPARC T4-1B, whose board layout (Figure 2) was modified and has only 2 hard disk drive slots versus 4 on the SPARC T3-1B. Another exception is that the SPARC T4-1 only supports 8 disk drive slots as compared to the 8 and 16 disk drive configurations supported by the SPARC T3-1.
The key components of the SPARC T4-1B are labeled along with the open space on the circuit board. The features and specifications of the SPARC T4 Servers are similar to that of the SPARC T3 Servers (Table 1).

<table>
<thead>
<tr>
<th>Processor</th>
<th>SPARC T4-1B</th>
<th>SPARC T4-1</th>
<th>SPARC T4-2</th>
<th>SPARC T4-4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size (RU)</td>
<td>server blade</td>
<td>2U</td>
<td>3U</td>
<td>5U</td>
</tr>
<tr>
<td>CPU sockets</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Max Memory (with 16-GB DIMM)</td>
<td>256 GBytes</td>
<td>256 GBytes</td>
<td>512 GBytes</td>
<td>1 TByte</td>
</tr>
<tr>
<td>I/O Slots / Protocol</td>
<td>2/4/PCIe2</td>
<td>6/PCIe2</td>
<td>10/PCIe2</td>
<td>16/PCIe2</td>
</tr>
<tr>
<td>1-GbE/10-GbE (for 10-GbE need FEM and NEM)</td>
<td>2/2</td>
<td>4/2</td>
<td>4/4</td>
<td>4/8</td>
</tr>
<tr>
<td>Max HDD</td>
<td>2</td>
<td>8</td>
<td>6</td>
<td>8</td>
</tr>
<tr>
<td>Recommended LDOMs</td>
<td>8*</td>
<td>8*</td>
<td>16*</td>
<td>32*</td>
</tr>
<tr>
<td>Service Processor chip/ SW</td>
<td>AST2200 / ILOM</td>
<td>AST2200 / ILOM</td>
<td>AST2200 / ILOM</td>
<td>AST2200 / ILOM</td>
</tr>
</tbody>
</table>

Table 1: SPARC T4 Servers Features and Specifications.

*Note: The maximum number of supported LDOMs is 128 but best practice recommendation is to have one LDOM per core.
The SPARC T4-1B uses the standard Constellation blade form factor while other three SPARC T4 servers are consistent with the SPARC T3 Server form factors. The number of processors on each server is the same as the number on their SPARC T3 Server counterparts. The maximum memory has increased to 2 times the capacity of the SPARC T3 Servers due to the new 16-GByte, 1066 MHz DIMMs.

The number of I/O ports on each SPARC T4 Server is basically the same as their SPARC T3 Server counterparts, but for some exceptions that have already been noted. As with its predecessor, the blade server has two PCIe2 interconnects connected to its dedicated ExpressModule slots and four PCIe interconnects connected to the two Network Express Module slots. The recommended number of LDOMs has changed. Due to best practices the maximum number of LDOMs matches the number of cores.

**SPARC T4-1 versus SPARC T3-1**
The SPARC T4-1 2U rack mount server uses the same chassis and I/O hardware as its predecessor, the SPARC T3-1. The motherboard and CPU supports the new Millbrook2 memory buffer or BoBs and the higher density 16-GByte DIMMs. The system firmware has been updated so review the product notes for the correct versions that are supported. The I/O expansion cards that are supported are basically the same except for some end-of-life deletions and post revenue release additions. The Aura card and the single ported Pallene card are not supported.

**SPARC T4-2 versus SPARC T3-2**
The SPARC T4-2 3U rack mount server also uses the same chassis and I/O hardware as its predecessor, the SPARC T3-2. The motherboard and CPU supports the new memory riser cards that contain the new Millbrook2 memory buffer BoBs and the higher density 16-GByte DIMMs.

**NOTE:** The new SPARC T4-2 memory riser cards are NOT interchangeable with the SPARC T3-2 memory riser cards on the SPARC T4-2 chassis.

There is support for mixed vendor power supplies that will be listed in system handbook, once the SPARC T4-2 releases. Review the product notes for the correct system firmware versions and for the supported I/O expansion cards. The Aura and single ported Pallene cards are not supported.

**SPARC T4-4 versus SPARC T3-4**
As with the other two servers, the SPARC T4-4 5U rack mount server uses the same chassis and I/O hardware as its predecessor, the SPARC T3-4. The processor module supports the new Millbrook2 memory buffer BoBs and the higher density 16-GByte DIMMs. The inter-CPU interconnect was improved for faster communications between the processors.

**NOTE:** The new SPARC T4 processor on the SPARC T4-4 server runs at 3.0 GHz.
NOTE: Mixing SPARC T4-4 and SPARC T3-4 processor modules in a SPARC T4 chassis is not supported.

The main module has a new FPGA that supports the SPARC T4 processor. As with the other servers, the SPARC T4-4 system firmware has been updated but the I/O expansion cards that are supported are the same except for some end-of-life deletions and post revenue release additions. The Aura and single-ported Pallene cards are not supported.

There is support for mixed vendor power supplies that will be listed in the system handbook, once the SPARC T4-4 releases. Review the product notes for the correct system firmware versions and supported I/O expansion cards.

SPARC T4-1B versus SPARC T3-1B
The SPARC T4-1B Constellation server blade motherboard layout is different than the SPARC T3-1B, though its components are similar. The CPU, memory and I/O changes discussed on the other SPARC T4 servers also exist on this blade. In addition, the number of disk slots is 2, as opposed to the 4 disk slots on the SPARC 3-1B.

As with the SPARC T3-1B, the SPARC T4-1B supports one CPU socket and 16 DIMM sockets. The REM supported is the Erie LSI SAS 2008 based card while the FEMs supported are the Sun Dual 10GbE FEM (Niantic) and the PCI-E pass through FEM (Nalia).

Architectural Differences between the SPARC T4 and SPARC T3 Processors
The main difference between these two servers is the processor chip each set of servers use. The SPARC T4 servers use the SPARC T4 processor chip, whose specifications are listed in Table 2, while the SPARC T3 servers use the SPARC T3 processor chip. Their specifications are listed in the table for a side-by-side comparison.

<table>
<thead>
<tr>
<th>Processor</th>
<th>SPARC T3</th>
<th>SPARC T4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>40nm</td>
<td>40nm</td>
</tr>
<tr>
<td># of cores</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td># of threads</td>
<td>128</td>
<td>64</td>
</tr>
<tr>
<td># of sockets</td>
<td>1-4</td>
<td>1-4</td>
</tr>
<tr>
<td>Core frequency (GHz)</td>
<td>1.65</td>
<td>2.85*</td>
</tr>
<tr>
<td>Execution pipelines per core</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Peak Instructions per cycle per core</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>FPUs per chip</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>I$ size (per core)</td>
<td>16KB</td>
<td>16KB</td>
</tr>
<tr>
<td>D$ size (per core)</td>
<td>8KB</td>
<td>16KB</td>
</tr>
<tr>
<td>L2$ size/Set Association</td>
<td>6MB/24-Way</td>
<td>128KB Dedicated Cache</td>
</tr>
</tbody>
</table>
Table 2: SPARC T4 and SPARC T3 Specifications

<table>
<thead>
<tr>
<th>L3$ size/Set Association</th>
<th>--</th>
<th>4MB/16-Way</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Type</td>
<td>DDR3</td>
<td>DDR3</td>
</tr>
<tr>
<td>I/O Bus</td>
<td>Two 8 lane PCIe2</td>
<td>Two 8 lane PCIe2</td>
</tr>
<tr>
<td>On-chip networking</td>
<td>Two 10-GbE interconnects</td>
<td>Two 10-GbE interconnects</td>
</tr>
<tr>
<td>Crypto Acceleration</td>
<td>RSA, int ECC, DES, 3DES, SHA384/512, AES, SHA, MD5, CRC32, Kasumi, and user land fast-path interface</td>
<td>ISA, DES, SHA1/256/512, AES, MD5, Kasumi, and Camellia</td>
</tr>
<tr>
<td>Single Socket Power (watts, watts / thread)</td>
<td>146, 1.1</td>
<td>219, 3.4</td>
</tr>
</tbody>
</table>

*Note, the SPARC T4-4 server has an effective clock speed of 3.0 GHz while the other servers have an effective clock speed of 2.85 GHz.

Both processors were produced using 40 nanometer technology but the big differentiator is the SPARC T4 processor core clock frequency of 2.85 GHz. This translates into a 4 to 5 times single thread execution advantage over that of the SPARC T3 processor.

**NOTE: The SPARC T4-4 server has an effective clock speed of 3.0 GHz while the other SPARC T4 servers have an effective clock speed of 2.85 GHz.**

The SPARC T3 processor still has an advantage in terms of the number of cores with each core having 8 threads for a maximum of 128 threads. But the SPARC T4 processor, with its 8 cores and 64 threads, can still outperform the SPARC T3 processor due to its single thread execution advantage.

Just like the SPARC T3 processor, the SPARC T4 processor supports one Floating Point Unit or FPU per core. There are some significant changes in the cache supported by the SPARC T4 processor. The data cache size per core was doubled to 16 Kbytes on the SPARC T4 processor while a new core Level 2 cache was added with 128 Kbyte dedicated cache along with a new 4MByte, 16-way associative Level 3 shared cache.

Both processors support DDR3 memory type with the same bandwidth but the SPARC T4 Servers will use new Millbrook2 memory buffers referred to as BoB2s and the DIMMs operate at a low voltage of 1.35 volts. No changes took place in terms of the processor’s I/O or on-chip networking as you can see in Table 2.

The SPARC T4 processor has also improved its encryption performance over the SPARC T3 by implementing it in hardware which results in a 10x performance increase over the software-only implementations and a 2x to 3x performance increase over current encryption hardware. The SPARC T4 processor implemented non-privileged bulk extensions for bulk-ciphers, secure hashes and public-key ciphers. The new encryption instructions have already been integrated into the SPARC T4 gate by the Solaris security group which supports the encryption standards listed in Table 2.
There was an increase in the power being consumed by the SPARC T4 processor, especially in the power consumed per thread, as listed in Table 2. Of course this significantly increases power consumption on the two and four socket servers.

**Memory Configuration Guidelines for the SPARC T4 Servers**

The memory configuration guidelines for each SPARC T4 Server are being covered here with key differences between the SPARC T4 and T3 noted.

**NOTE: The SPARC T4 Servers will not support mixed memory DIMM sizes which was supported on the SPARC T3 Servers.**

**SPARC T4-1**

The SPARC T4-1 memory configuration guidelines are:

- There are a total of 16 slots that support DDR3 DIMMs.
- Three DIMM capacities are supported: 4 GBytes, 8 GBytes, and 16 GBytes
- The DIMM slots are organized into four branches, with each branch connected to a separate Buffer-on-Board ASIC. These branches are shown in the Figure 3 as BOB0 through BOB3.
- Each BOB ASIC supports two DIMMs through separate DDR3 channels.
- The DIMM slots may be populated as 1/4 full, 1/2 full, or full. Use Figure 3 as a guide for populating the DIMM slots.
  - 1/4 Full -- Install DIMMs in the slots labeled 1 only.

**NOTE: The SPARC T4 Server must have at least a 1/4-full memory configuration.**

- 1/2 Full -- Install DIMMs in the slots labeled 1 and 2 only.
- Full -- Install DIMMs in every slot (1, 2, and 3).
- All DIMMs in the server must be the same in the following characteristics:
  - DIMM size -- All DIMMs must have the same capacity (all 4-GByte, all 8-GByte, or all 16-GByte).
  - DRAM type -- The memory organization on all DIMMs must be either 1-GByte or 2-GByte.
  - Rank -- All DIMMs must have the same number of ranks.
  - Architecture -- All DIMMs must use either x4 or x8 memory organization.
- Any DIMM slot that does not have a DIMM installed must have a DIMM filler

**NOTE: If the server’s memory configuration fails to meet any of these rules, applicable error messages are reported. See “DIMM Configuration Error Messages” within SPARC T4-1 Service Manual for their description.**
SPARC T4-2

The SPARC T4-2 riser population rules are listed here with the corresponding Figure 4:

- A maximum of two memory risers (numbered MR0 and MR1) are supported per CPU, thus allowing up to four memory risers.
- Each memory riser slot in the server chassis must be filled with either a memory riser or filler panel, and each memory riser must be filled with DIMMs and/or DIMM filler panels. For example, empty CPU sockets (P1 and P3) must have associated memory riser slots populated with two riser filler panels per CPU.
- Performance-oriented configurations should be configured with two memory risers per CPU. In configurations that do not require two memory risers per CPU, the following guidelines should be followed:
  - Populate riser slot MR0 for each CPU, starting with the lowest numbered CPU (P0).
  - Populate riser slot MR1 for each CPU, starting with the lowest numbered CPU (P0).
The SPARC T4-2 memory performance guidelines are:

- For maximum bandwidth, install eight DIMMs in each memory riser.
- The more DIMMs you install on each memory riser, the higher the memory bandwidth. If a memory riser has only four dual-rank DIMMs, its bandwidth is approximately 94% of the possible maximum. If a memory riser has only two dual-rank DIMMs, its bandwidth is approximately 29% of the possible maximum. Accordingly, a memory riser with four 4-GB DIMMs has a much higher bandwidth than a memory riser with two 8-GB DIMMs.
- To decrease latency, balance memory risers by installing the same configuration of DIMM sizes on the MR0 and MR1 risers for each CPU. When MR0 and MR1 have similar DIMM configurations, for each CPU in the system, the system enables an interleaving optimization that reduces memory latency for large workloads.

**SPARC T4-4**

The SPARC T4-4 DIMM configuration guidelines for the processor modules are:

- There are a total of 32 slots that support DDR3 DIMMs within each processor module.
- There are three supported DIMM capacities: 4 GByte, 8 GByte, and 16 GByte.
- The DIMM slots are organized into four branches, with each branch connected to a separate Buffer-on-Board (BOB) ASIC. The four branches are designated BOB0 through BOB3.
- Each BOB ASIC has two DDR3 channels, with each channel supporting two DIMMs. These configuration details are illustrated in Figure 5 in the following topics.
- DIMM slots that do not have a DIMM installed must have DIMM fillers plugged into the sockets.
- Sixteen of the 32 DIMM slots (four banks of four DIMM slots) are associated with CMP0, and the other sixteen DIMM slots are associated with CMP1. Figure 5 shows which DIMM slots are associated with each CMP.

**NOTE:** The Half and Full configuration are described in detail within the “DIMM Configuration Guidelines” section within the SPARC T4-4 Service Manual.
SPARC T4-1B

The SPARC T4-1B DIMM configuration guidelines are:

- Use only supported industry-standard DDR-3 DIMMs.
- Use supported DIMM capacities: 4 Gbyte, 8 Gbyte, and 16 Gbyte. Refer to the SPARC T4-1B Server Module Product Notes for the latest information.
- You can install quantities of 4, 8, or 16 DIMMs, following color-coded DIMM sockets listed in Figure 6:
  - 4 DIMMs: White sockets
  - 8 DIMMs: White sockets and black sockets with white ejectors
  - 16 DIMMs: Fill all sockets
- All DIMMs must have the same part number.

![DIMM physical locations](image)

Legend:

1. Fault Remind button
2. Fault Remind Power LED
3. DIMMs controlled by BOB3:
   - /SYS/MB/CMP0/ CH0/D1 (DIMM Quantity=16)
   - /SYS/MB/CMP0/ CH0/D0 (DIMM Quantity=8 or16)
   - /SYS/MB/CMP0/ CH1/D1 (DIMM Quantity=16)
   - /SYS/MB/CMP0/ CH1/D0 (DIMM Quantity=4)
4. DIMMs controlled by BOB2:
   - /SYS/MB/CMP0/ CH0/D1 (DIMM Quantity=16)
   - /SYS/MB/CMP0/ CH0/D0 (DIMM Quantity=8 or16)
   - /SYS/MB/CMP0/ CH1/D1 (DIMM Quantity=16)
   - /SYS/MB/CMP0/ CH1/D0 (DIMM Quantity=4)
5. DIMMs controlled by BOB0:
   - /SYS/MB/CMP0/ CH0/D1 (DIMM Quantity=16)
   - /SYS/MB/CMP0/ CH0/D0 (DIMM Quantity=8 or16)
   - /SYS/MB/CMP0/ CH1/D1 (DIMM Quantity=16)
   - /SYS/MB/CMP0/ CH1/D0 (DIMM Quantity=4)
6. DIMMs controlled by BOB1:
   - /SYS/MB/CMP0/ CH1/D0 (DIMM Quantity=4)
   - /SYS/MB/CMP0/ CH1/D1 (DIMM Quantity=16)
   - /SYS/MB/CMP0/ CH0/D0 (DIMM Quantity=8 or16)
   - /SYS/MB/CMP0/ CH0/D1 (DIMM Quantity=16)
7. DIMM Fault LEDs
Software Differences between the SPARC T4 and SPARC T3 Servers

Some of the software components of the SPARC T4 Servers, that are displayed in the software block diagram in Figure 7, have been modified for this new platform.

Listed here are the software and firmware components that were affected and the changes that took place.

**OBP**

Within OBP there are very few customer identifiable changes other than SPARC T4 banner changes and version changes. Check the product notes for the OBP version with which each server was released. As you look closer there are some configuration rule changes that are significant.

1. An odd core can only be enabled if its even sister core is enabled and available. This is required due to T4 clock routing. For example:

   Example: /SYS/P00/CM00/CORE2 disabled:
   [CPU 0:0:0] ERROR: /SYS/P00/CM00/CORE2: Not configured (Required L2 Cache is disabled)
   [CPU 0:0:0] ERROR: /SYS/P00/CM00/CORE3: Not configured (Required Core 2 is not configured)
2. L1 Cache, Data Cache and L2 Cache can be ASR disabled. The core availability depends on the cache state. For example:

Example: /SYS/PM0/CMP0/CORE3/L1CACHE disabled:
[CPU 0:0:0] ERROR: /SYS/PM0/CMP0/CORE3: Not configured (Required L1 Dcache is disabled)

**POST**

POST for the SPARC T4 Servers is highly leveraged from the SPARC T3 Servers. The key addition to T4 POST was L2 and L3 cache test coverage, which was provided by hostconfig (MBIST) that is resident in OBP. These tests are enabled earlier on SPARC T4 Servers before POST starts utilizing memory.

**ILOM**

The SPARC T4 Servers will release with ILOM version 3.0.16 (check the product notes to verify). There are a few ILOM related changes that have taken place since ILOM 3.0.12 released with the SPARC T3 Servers other than minor bug fixes. One of the changes is the new part numbering style. This can be seen in the ILOM show command displayed here:

For the SPARC T3-1 Server:  
```
show /SYS
product_name = SPARC T3-1
product_part_number = 602-4916-03
```

For the SPARC T4-1 Server:  
```
show /SYS
product_name = SPARC T4-1
product_part_number = 7912345-2
```

The majority of the changes are platform related. The following is a list of these changes:

1. Support for lower-voltage (1.35V) DDR3 DIMMs
2. Support for fewer cores in the ILOM inventory
3. Support for faulting and disabling L1 cache/Instruction cache, L1 cache/Data cache and L2 cache within ILOM inventory.
4. Support for ILOM logging of L3 cache ereports
5. Support for ILOM generation of a fault when a processor module is installed in a T4 slot and is reported in CR 7080792 for the SPARC T4-4. It is currently closed as a “will not fix”.
6. Warning messages will be generated if the memory DIMMs are not the same size.
**Solaris**

The SPARC T4 Servers will support Solaris 10 Update 10 along with patches (check for these patches in the product notes) as well as Solaris 11 Build 173 (check this in the product notes to verify the released version). Solaris 10 Updates 8 and 9 are also supported with the proper maintenance updates but they will not be factory pre-installed on the SPARC T4 servers.

Some additions to Solaris in support of the SPARC T4 Servers are:

1. **PSARC 2010/425 Solaris support for the SPARC T4 platforms**
2. **Support for new T4 crypto instructions**
3. **Support for new 2GB HW page size integrated but disabled (7018576, 7024586)**
4. **New SPARC T4 performance counters via cpustat(1M), cputrack(1)**
5. **New hardware capabilities (hwcaps) reported by isainfo –x**

   # isainfo –x
   sparcv9: crc32c cbcond pause mont mpmul sha512 sha256 sha1 md5 camellia kasumi des cspare ima
   hpc vis3 fmaf asi_blk_init vis2 vis popc

   sparc: crc32c cbcond pause mont mpmul sha512 sha256 sha1 md5 camellia kasumi des cspare ima
   hpc vis3 fmaf asi_blk_init vis2 vis popc v8plus div32 mul32

6. **New output for prtdiag and psrinfo commands (Note: the MHz ratings are not up to date).**

   # prtdiag
   System Configuration: Oracle Corporation sun4v SPARC T4-1
   Memory size: 7680 Megabytes
   -------------------------------- Virtual CPUs --------------------------------
   CPU ID Frequency Implementation Status
   ------- ------- ------------------ --------
   0 2548 MHz SPARC-T4 on-line
   1 2548 MHz SPARC-T4 on-line
   2 2548 MHz SPARC-T4 on-line
   3 2548 MHz SPARC-T4 on-line
   4 2548 MHz SPARC-T4 on-line
   5 2548 MHz SPARC-T4 on-line
   6 2548 MHz SPARC-T4 on-line
   7 2548 MHz SPARC-T4 on-line
   8 2548 MHz SPARC-T4 on-line

   # psrinfo –vp
   The physical processor has 8 cores and 64 virtual processors (0-63)
   The core has 8 virtual processors (0-7)
   The core has 8 virtual processors (8-15)
   The core has 8 virtual processors (16-23)
   The core has 8 virtual processors (24-31)
   The core has 8 virtual processors (32-39)
   The core has 8 virtual processors (40-47)
   The core has 8 virtual processors (48-55)
   The core has 8 virtual processors (56-63)
   SPARC-T4 (chipid 0, clock 2548 MHz)

7. **Support for the new cpu module SPARC-T4**
8. **New performance counter module pcbe.SPARC-T4**
9. **New kernel binaries:**
   - /platform/sun4v/lib/sparcv9/libc_psr/libc_psr_hwcap3.so.1
   - /platform/sun4v/lib/sparcv9/libc_psr/libc_psr_hwcap3.so.1
   - /platform/sun4v/kernel/misc/sparcv9/sha1
   - /platform/sun4v/kernel/misc/sparcv9/sha2
   - /platform/sun4v/kernel/crypto/sparcv9/aes
   - /platform/sun4v/kernel/crypto/sparcv9/aes256
   - /platform/sun4v/kernel/crypto/sparcv9/des
10. Diagnosis of faults in directly attached disks
11. Ability to retire an individual line of L2 or L3 cache, rather than offline all cpu threads associated with the affected cache. Small numbers of cache lines can be retired without significant effect on system performance, resulting in higher availability due to less downtime for service calls.

Drivers and Utilities
The SAS disk controller driver is the mpt_sas which uses WWID paths within Solaris. The disk drives, using this driver, can be moved from slot to slot and still be able to boot. For more information about the onboard LSI 2008 controller or the REM LSI 2008 controllers refer to: http://www.lsi.com/support/sun. The RAID utility, SAS2ircu, can be used to configure RAID groups. The supported RAID levels on the onboard LSI 2008 controllers and the REM LSI 2008 controllers are 0, 1 and 1E. The SG-SAS6-EM-Z HBA ExpressModule also supports RAID 0, 1 and 1E.

NOTE: On the SPARC T4-1B, support for RAID 1E requires the Sun Blade Storage Module M2 and there is no REM card that supports RAID 5, 6 or any other higher level.

The pre-boot configuration can be configured using OBP/Fcode commands such as: show-children, show-volumes, create-raid0-volume, create-raid1-volume, create-raid1e-volume, delete-volume and activate-volume.

The network drivers for FEM cards using specific NEMs are listed in Table 3.

<table>
<thead>
<tr>
<th>FEM</th>
<th>NEM</th>
<th>Drivers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sun Dual 10GbE FEM (Niantic)</td>
<td>(Opus)</td>
<td>ixbge (10GbE)</td>
</tr>
<tr>
<td>PCI-E pass through FEM (Nalia).</td>
<td>(SOL)</td>
<td>igb (1GbE), sxge (10GbE)</td>
</tr>
<tr>
<td>PCI-E pass through FEM (Nalia).</td>
<td>(Hydra2)</td>
<td>igb (1GbE), hxge (10GbE)</td>
</tr>
</tbody>
</table>

Table3: FEM and NEM Drivers

Servicing and Maintenance Differences between the SPARC T4 and T3 Servers
Because there are few if any physical and feature differences between the SPARC T3 and SPARC T4 Servers you would not expect any significant differences in their service and maintenance procedures. That does not mean that they will share the same technical manuals. Each SPARC T4 Server will each have an Installation Guide and a Service Manual that you
can access from the System Handbook (https://support.oracle.com/handbook_private/index.html) once they are posted.

Due to their similarities, you may think that the SPARC T3 Server can be upgraded to run as a SPARC T4 Server, but as we have discussed, there are some differences that will not permit a field upgrade.

**NOTE: The SPARC T3 Servers will NOT be field upgradeable to SPARC T4 Servers.**

**Troubleshooting Differences between the SPARC T4 and T3 Servers**

The data collectors and diagnostic tools used for the SPARC T3 Servers will also be used for the SPARC T4 Servers which includes OBP, ILOM, IPMI, SunVTS and Solaris FMA. All these tools are continued to be used though you should check the product notes for their minimum supported versions.

Electronic Prognostics (EP) is a new facility being introduced on the SPARC T4 Servers. It performs an analysis of time series telemetry data collected from the physical and logical sensors in the system. It aids in online analysis by looking for leading indicators of failure by monitoring learned relationships among various sensors. Any anomalies in the learned relationships may be indications of a likely failure which can give a much earlier indication than the traditional threshold-based approach used with individual sensors. It also aids in offline analysis by providing data for root cause analysis and saves data like a black-box recorder (BBR) which can show the states of the system leading up to the failure.

EP is integrated within the service processor firmware and deployed as a layered product within the host components, as you can see in Figure 8.
The data recorded on the BBR is saved in a fixed size file that uses Oracle-patented “Zeno’s Circular File” structure to retain a lifetime history of telemetry in a finite storage footprint. The BBR is divided into two segments. The current buffer records each telemetry sample in the file while the historical buffer statistically compresses older telemetry data. No data is removed. As the data gets older it is summarized over greater intervals.

EP will come pre-installed on the SPARC T4 Server along with Solaris 10 or 11 and LDOM 2.1. The detectors implemented at GA of the SPARC T4 Servers are: CPU Vcore degradation detector, DC/DC converters degradation detector and the CPU heatsink dust buildup detector. Additional detectors will be added during the life of the platform.